Notice of Allowability	Application No.	Applicant(s)	
	09/931,848	GALZUR ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed on 5/4/2005 and phone interview of 6/9/2005*.

2. ☒ The allowed claim(s) is/are *5,6,8-13 and 16-18*.

3. ☒ The drawings filed on *9 August 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOSE CABRERES
PRIMARY EXAMINER

DETAILED ACTION

1. Claims 5, 6, 8-14, 16-18 and 20 are pending and have been examined. Claims 14 and 20 have been canceled through the Examiners Amendment detailed therein.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone message left by Attorney Patrick Bever on June 23, 2005 at 3:12 pm EST.

Please amend the application as follows:

As per Claim 8:

On line 3, please change "array" first occurrence to "device".

As per Claim 11:

On line 3, please change "array" first occurrence to "device".

As per Claim 12:

On line 3, please change "array" first occurrence to "device".

As per Claim 13:

On line 3, please change "array" first occurrence to "device".

As per Claim 16:

On line 3, please change "array" first occurrence to "device".

As per claims 14 and 20:

Please cancel claims 14 and 20.

Response to Arguments

3. Applicant's arguments, see Applicant Remarks, filed 5/4/2005, and phone interview on 6/9/2005 with respect to claims 5, 6, 8-13, and 16-18 have been fully considered and are persuasive. The Examiner has withdrawn the rejection of claims 5, 6, 8-13, and 16-18.

Allowable Subject Matter

4. Claims 5 and 6 are allowed. Please refer to Final Office Action paper number 12282004 for Reason For Allowance for these claims.

5. Clams 8-13, and 16-18 are allowed.

The following is an Examiner's Statement of Reasons for Allowance:

The present invention pertains generally to a method and structure for performing wafer sort tests on an EEPROM circuit including an array of 2-bit non-volatile memory cells. The claimed invention (claim 8 as representative, claim 8 is the broadest of the independent claims) recites features such as:"... storing a series of self-test instructions transmitted from the tester in the first array of the non-volatile memory device, the series of self-test instructions including a first instruction and a second instruction; reading the first instruction from the first array and transferring the first instruction to a command

register of the control circuit, wherein the first instruction includes a pre-determined data pattern; writing the predetermined data pattern to a second array of non-volatile memory cells in accordance with the first instruction stored in the command register; and storing a first address code transmitted from the tester."

The prior arts of record teach a non-volatile memory array where algorithmic parameters are stored in non-user addressable locations (first array) Electrically Erasable Array 46 and data values are stored in another area of the array (second array) as well as an entry/exit control unit 40 (control circuit) for receiving externally applied test parameter (self-test instructions) from an external tester. The prior arts of record also teach storing a series of self-test instructions transmitted from the tester; reading the first instruction from the first array; and writing the predetermined data pattern to a second array as set forth in claims 8, 11-13 and 16; Jang et al. (US-5640354) is one example of such prior arts.

The prior arts of record, however, fail to teach, singly or in combination, the method of reading the first instruction by transmitting the first address code to the addressing circuit and reading the first instruction from the first array per claim 8, transferring the second instruction from the first array to the command register of the control circuit, the second instruction including a predetermined data pattern; and reading data values from the second array of non-volatile memory cells in accordance with the second instruction; and comparing the data values read from the second array with the predetermined data pattern stored in the command register per claim 11, and wherein storing the series of self-test instructions comprises writing the series self-test

instructions into sequentially addressed non-volatile memory cells of the first array, wherein the method further comprises storing a first address code transmitted from the tester in a counter, wherein reading the first instruction includes transmitting the first address code from the counter to an addressing circuit, whereby the addressing circuit accesses and reads the first self-test instruction from the first array, and wherein reading the second instruction includes incrementing the counter to generate a second address code, and transmitting the second address code from the counter to the addressing circuit per claim 12. The prior arts of record also fail to teach, singly or in combination, storing a start self-test command transmitted from the tester the command register, wherein the first instruction is read from the first array in response to the stored start self- test command per claim 13 and reading the self-test instruction includes transmitting the address code to an addressing circuit, whereby the addressing circuit accesses and reads the self-test instruction from the first array per claim 16. The Applicant amended claims 8 and 11-13 to incorporate the subject matter of canceled base claim 7, thus placing claims 8-13 in condition for allowance. Claim 16 is amended to incorporate the subject matter of canceled base claim 15, thus placing claims 16-18 in condition for allowance. As a result the Examiner favors the allowance of claims 8-13, and 16-18.

Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

6/28/05

JOSEPH TORRES
PRIMARY EXAMINER